

DECAL

A RECONFIGURABLE CMOS SENSOR FOR PRE-SHOWER, OUTER TRACKING AND DIGITAL EM CALORIMETRY IN FUTURE COLLIDERS

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CPAD 2021

Stony Brook University

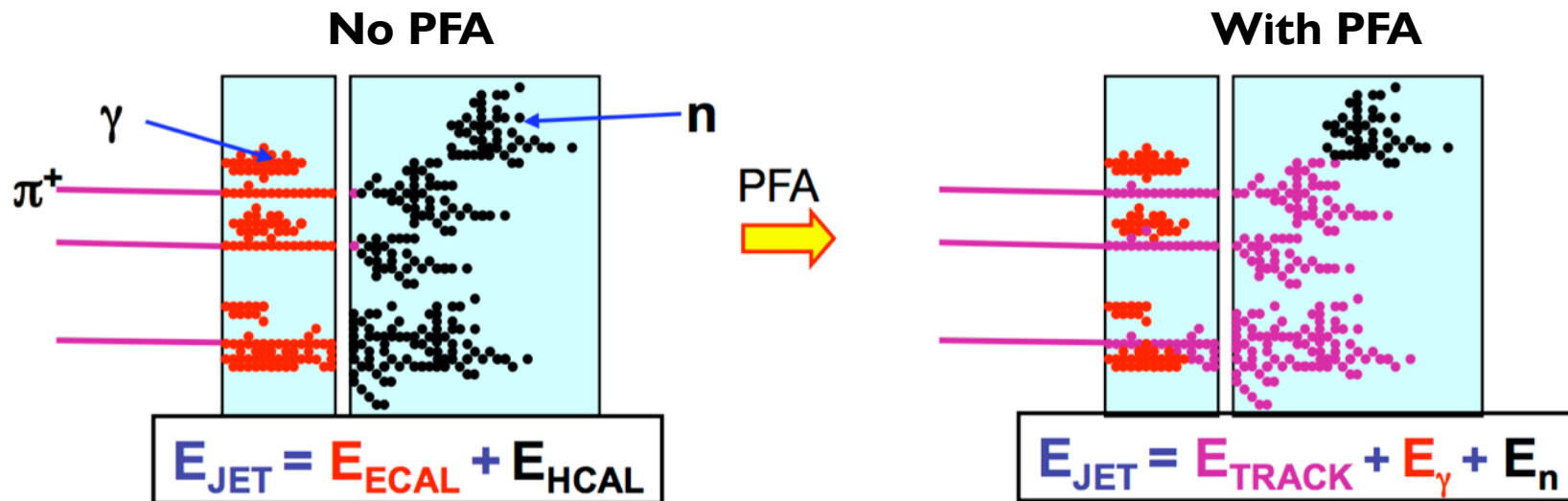
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- High granularity calorimetry
 - SiW calorimetry
 - Digital ECAL
- Simulation
 - Previous results – energy resolution
 - Ongoing work – particle reconstruction
- DECAL chip
 - TowerJazz 180 nm DMAPS
 - Results with 1st DECAL prototype
 - Preliminary results with new DECAL FD prototype

High granularity calorimetry

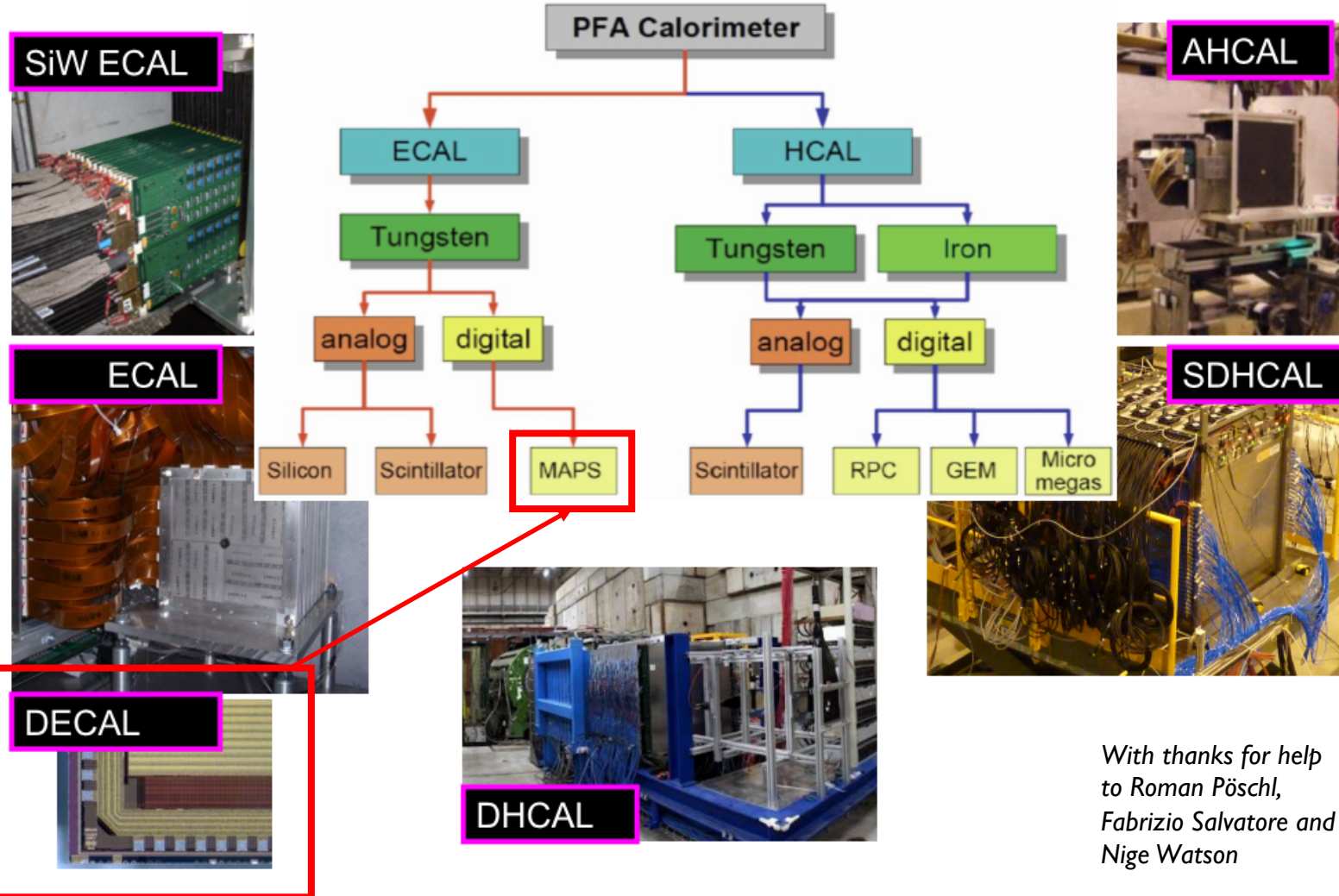
High granularity calorimetry offers the possibility of using Particle Flow Analysis (PFA) techniques to make best use of all detectors to measure jet energies

- Can associate ECAL hits/clusters with specific tracks and measure each particle within a jet with the appropriate calorimeter
 - Charged tracks = Tracker
 - e/photons = ECAL
 - Neutral hadrons (only 10%) = HCAL



CALICE collaboration

- CALICE: R&D group of around 300 physicists and engineers working to develop new, high performance detectors for high energy e^+e^- experiments (<https://twiki.cern.ch/twiki/bin/view/CALICE/WebHome>)
- SiW calorimetry has long been under consideration as an option within the CALICE collaboration as offering unprecedented granularity for PFA and is the focus of extensive prototyping and test beam activities



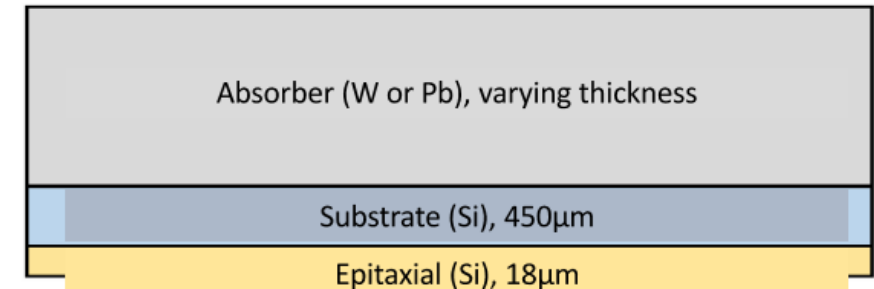
With thanks for help
to Roman Pöschl,
Fabrizio Salvatore and
Nige Watson

SiW Calorimetry

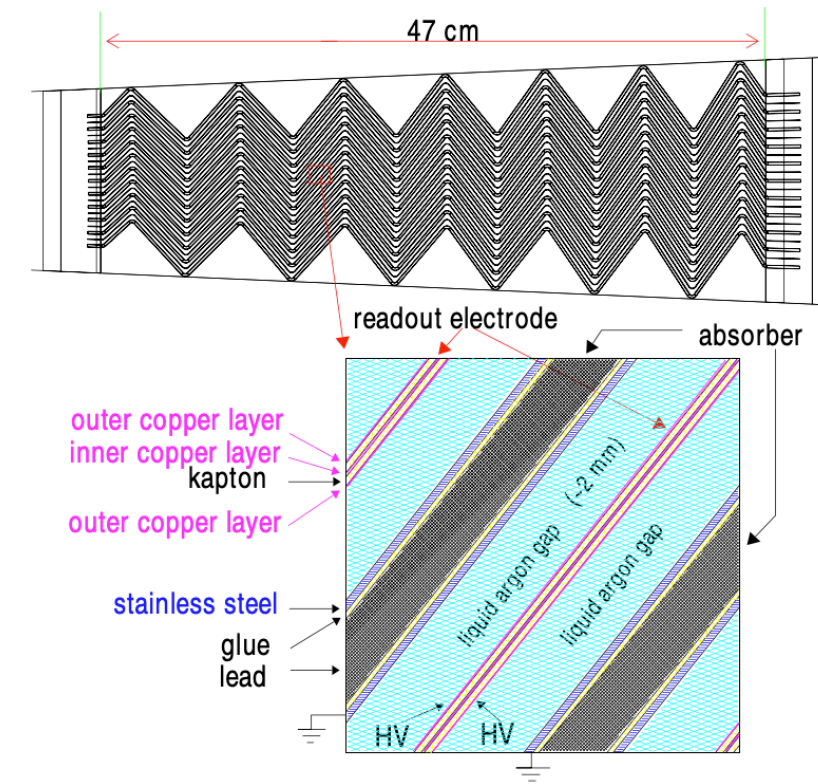
SiW calorimetry: alternating layers of absorbing W and sensing Si layers

- SiW Advantages in comparison to LAr systems:
 - PFA – potentially even better with CMOS
 - Lower ratio of sensing material -> **Compact calorimeter ~20 cm thick** (esp. if contained in solenoid) -> **decreased overall detector volume and costs**
- Disadvantages:
 - Cost of ECAL itself
 - Current costs estimates of hybrids are high and cost of CMOS has potential to be cheaper for large areas
 - Radiation hardness (FCC-hh forward calo)
 - EM energy resolution (wrt eg ATLAS and CMS)

SiW



LAr (ATLAS)



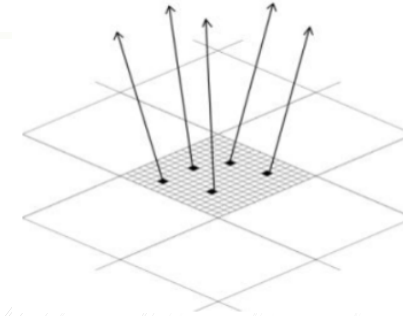
Digital SiW EM calorimetry

Digital calorimetry with MAPS

- Basic idea: count # of pixels above threshold to estimate the shower energy
- Pixel size must be small to avoid saturation (more than 1 hit/pix) in high-density showers

Why digital Si?

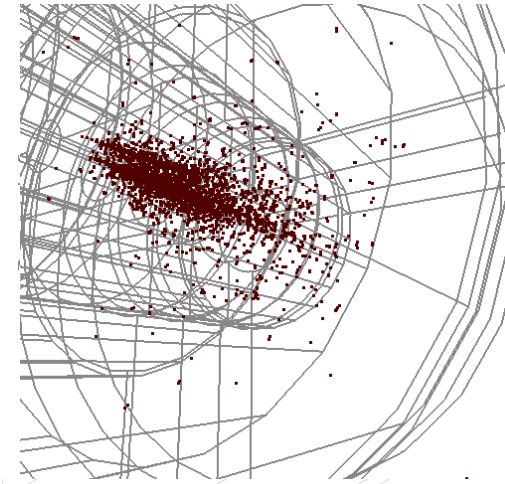
- Production costs of CMOS may decrease with growing market to be cheaper than hybrid sensors
- Full-system complexity and costs can be lower due to integration of sensor and electronics
- Potential to improve reconstruction if increased granularity can be exploited (50 μm crossed strips vs. 5 mm pads)
 - On-going simulation work on this front with $\pi^0 \rightarrow \gamma\gamma$ reconstruction
- MAPS prototypes in 150 nm and 180 nm CMOS imaging process have demonstrated radiation hardness above $1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$



CLIC simulations, 50 GeV $\pi^0 \rightarrow \gamma\gamma$
Digital, 50 μm granularity

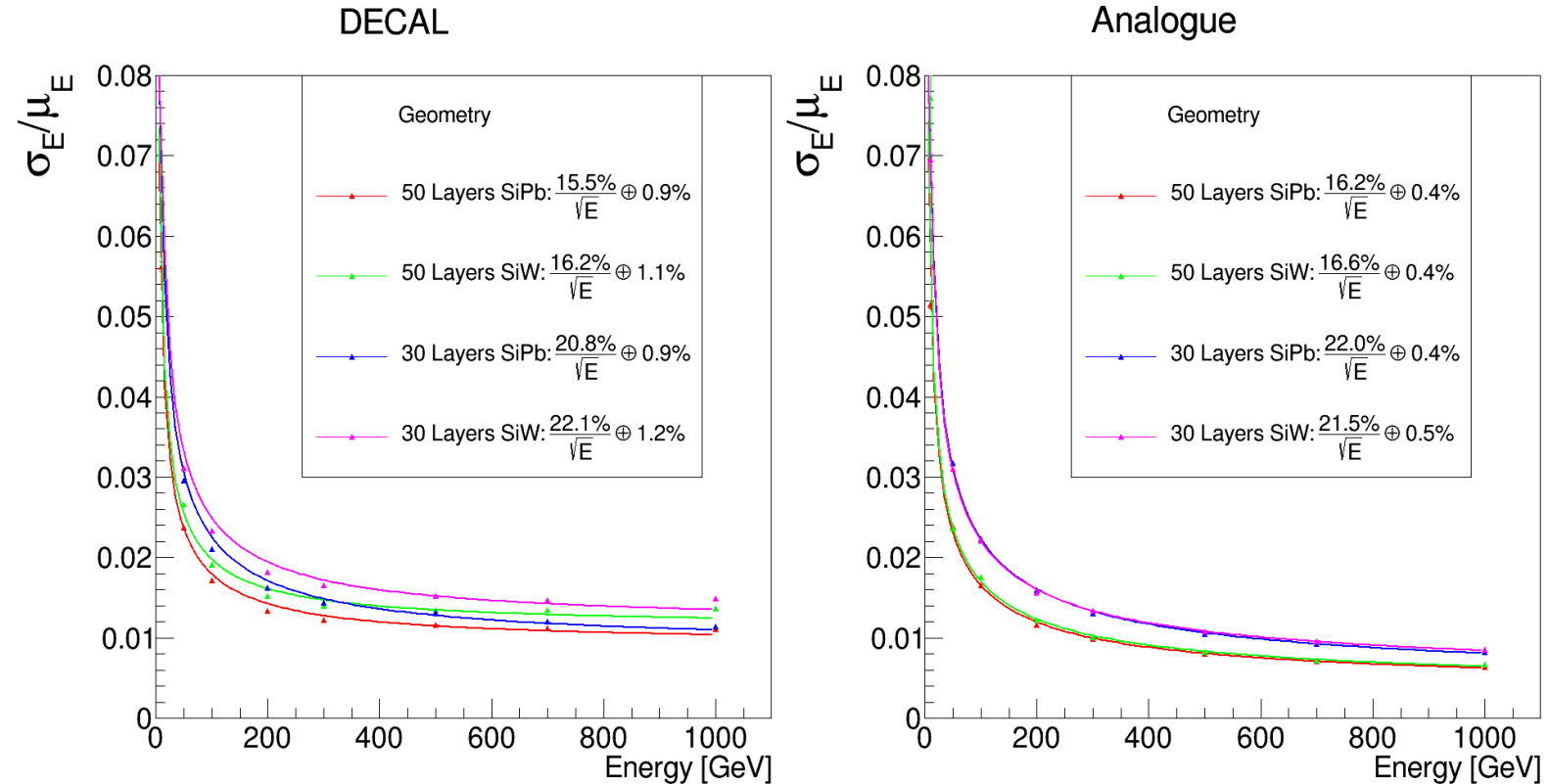
Analog, 5 mm pads

NB markers are in pixel center, not pixel size



Simulation results – energy resolution

- For single electrons, similar performance of Digital ECAL (with realistic channel threshold per pixel of $480e^*$) and Analogue ECAL (with perfect performance and full substrate signal per pad) up to around 300GeV (4T field without pile-up)
- Above this energy, saturation (more than one hit per $50\mu\text{m} \times 50\mu\text{m}$ pixel) starts to impact performance of digital compared with analogue ECAL
- Simulation work focused on reconstruction of $\pi^0 \rightarrow \gamma\gamma$ with PFA is on-going



CLICDP MEETING (27/08/2019) ROBERT BOSLEY

* $6 \times \sigma$ assuming noise of $\sigma = 80e$

The DECAL sensor

TowerJazz 180 nm CMOS imaging process

- Same process as ALPIDE chip in ALICE

64x64 matrix of **55 x 55 μm pixels**

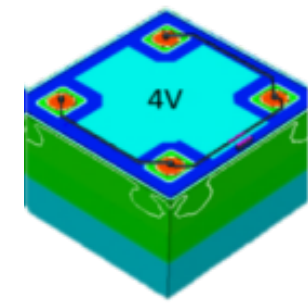
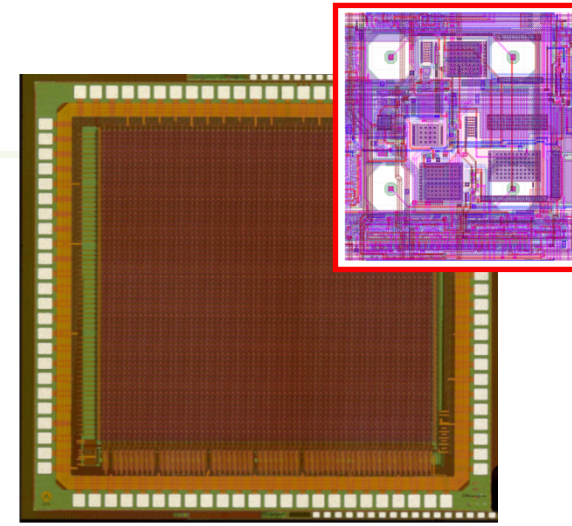
- 4 collection electrodes in pixel corners with low capacitance
- Pre-amp, shaper, & comparator with trimming DAC
- 40 MHz readout
- A single analog test pixel – only digital readout from rest of the matrix

Reconfigurable sensor as:

- 5mm x 55 μm strips (for pre-shower and outer tracking)
 - Better resolution than pad mode
 - Counts up to 3 hits/strip
- 5mm x 5mm pad
 - Counts up to 15 hits/strip

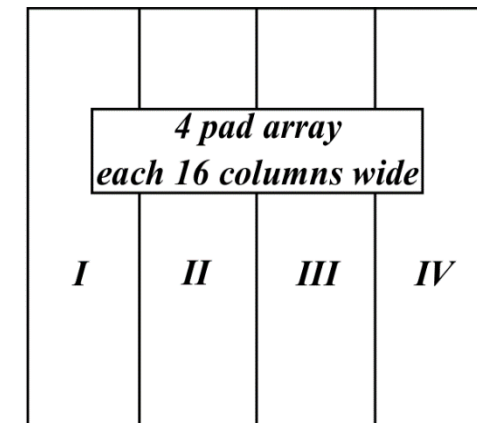
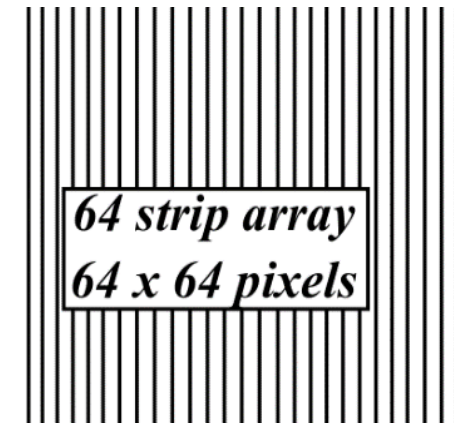
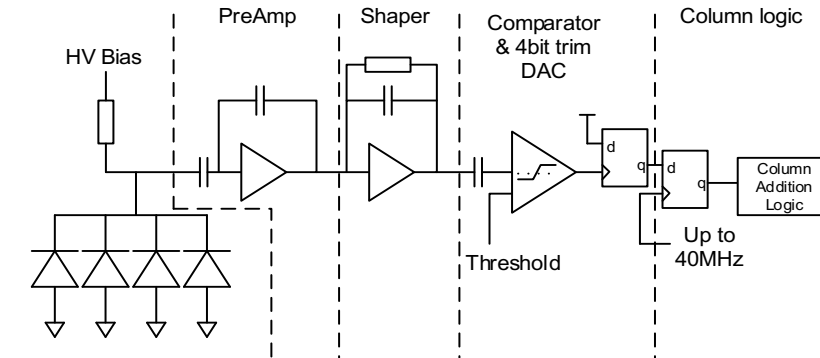
2nd prototype: DECAL FD

- now in **modified TowerJazz** process for **improved radiation hardness and fast charge collection**
 - Same process as used for MALTA and TjMonoPlx (Pernegger et al. NIM A 924 2019 92-98)



4 Diode TCAD Simulation: Giulio Villani

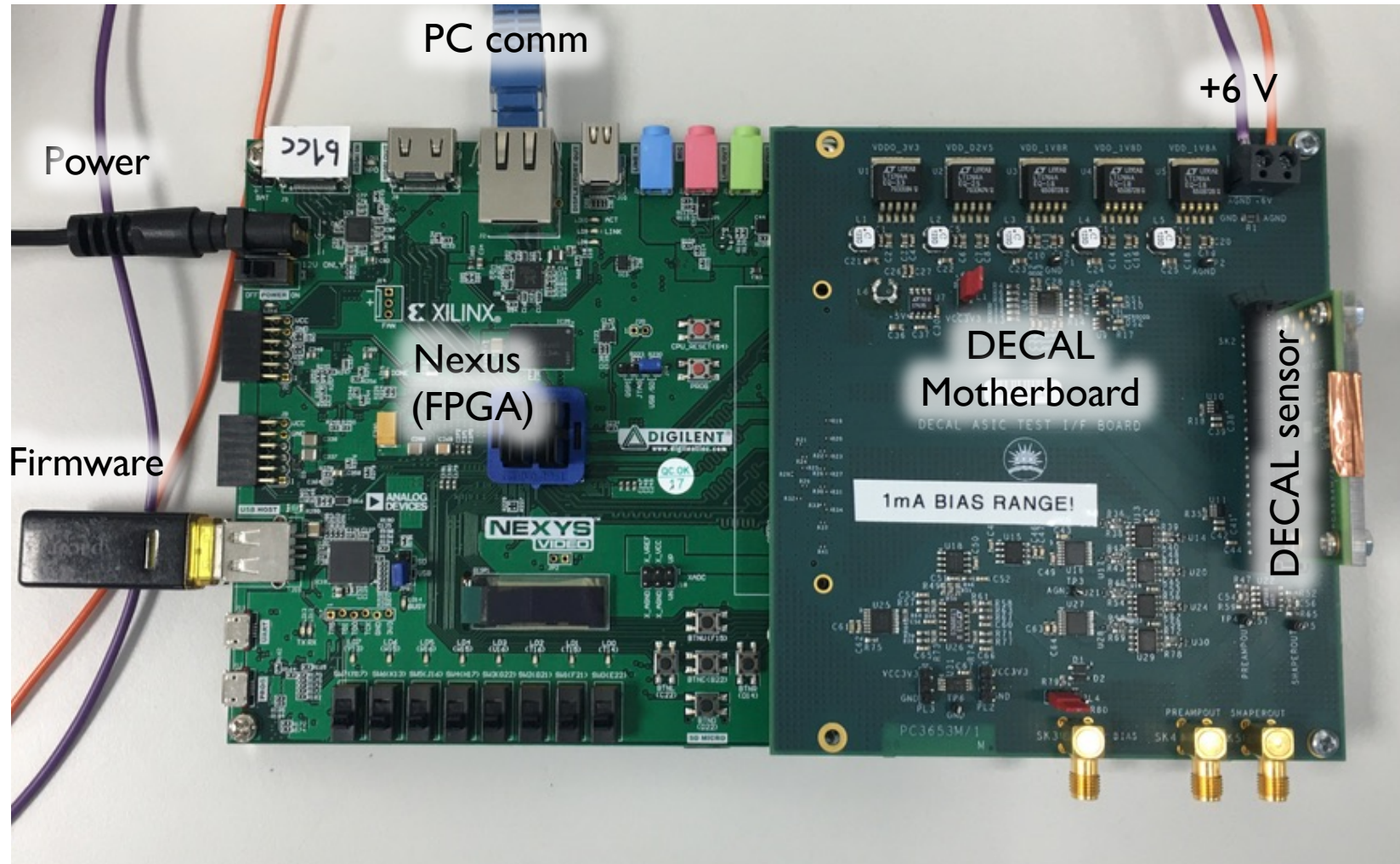
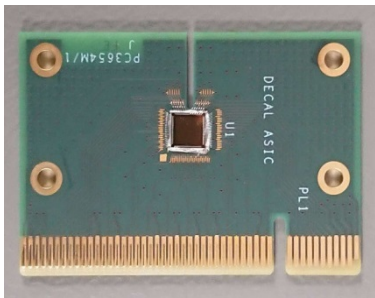
TWEPP (4/9/19) S.BENHAMMADI



DECAL Data Acquisition

- DIGILENT NEXYS Video Board
- DECAL motherboard for software-controlled biasing
- ATLAS ITSDAQ data acquisition software
- 40 MHz readout

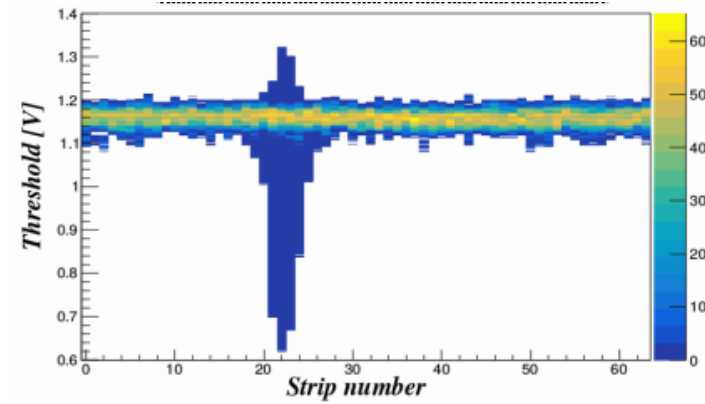
DECAL on carrier board



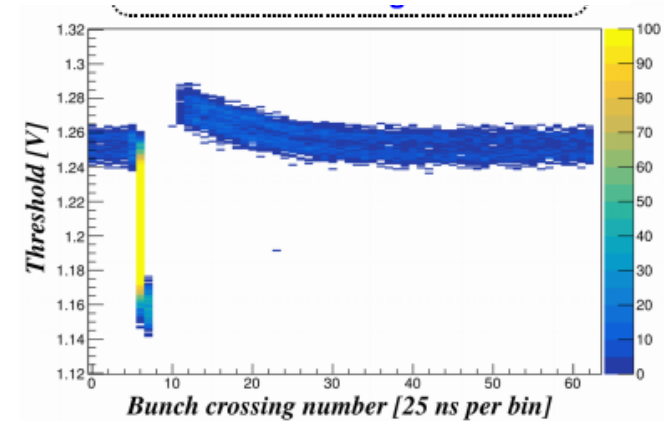
DECAL laser measurements

- Measurements with first version of DECAL and 1064 nm IR laser
- Unfocused laser spot and shaper output measured digitally
- Strip and pad mode counting logic tested
- Analog output tested

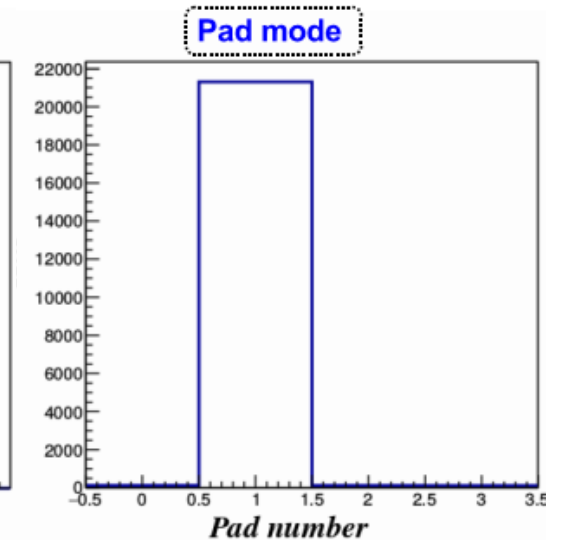
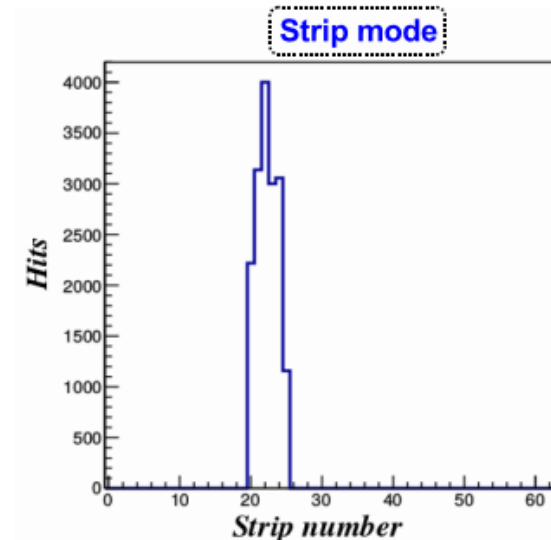
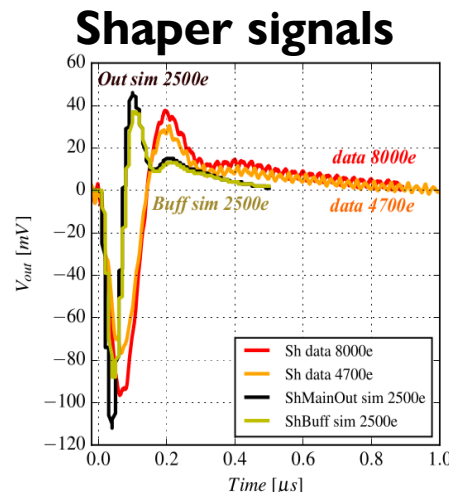
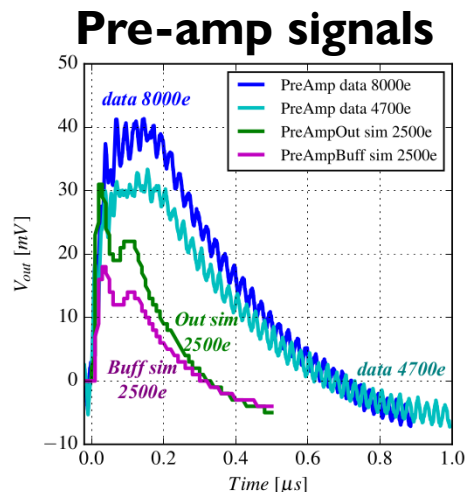
Threshold at which output of comparator first fires vs strip #



Single strip threshold at which comparator first fires vs time



IEEE MIC-NSS (30/10/19) I. Kopsalis



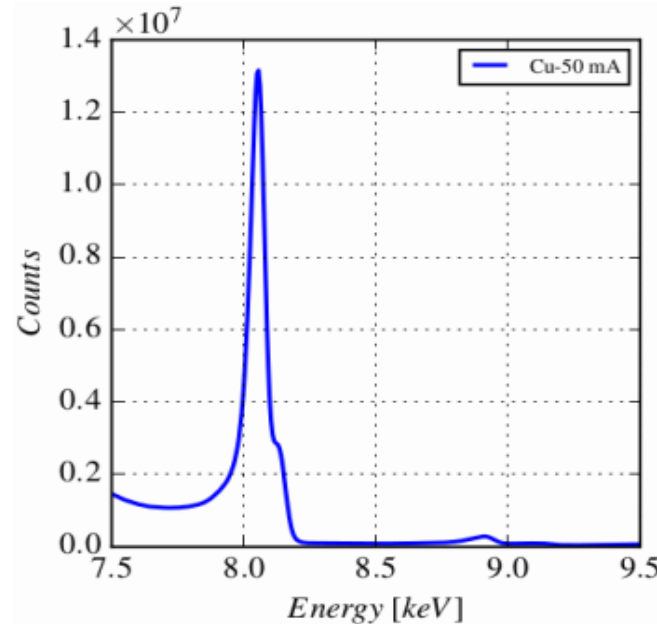
DECAL Cu calibration



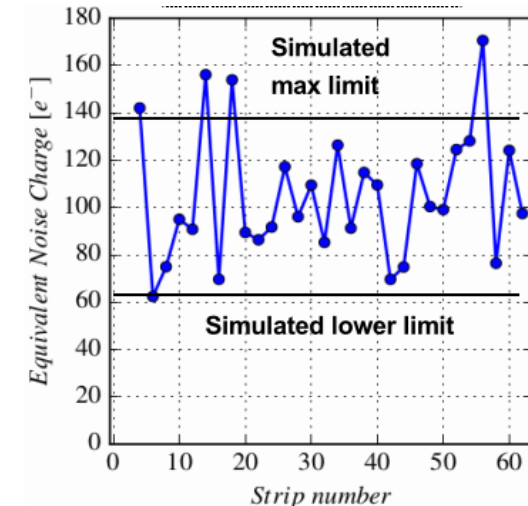
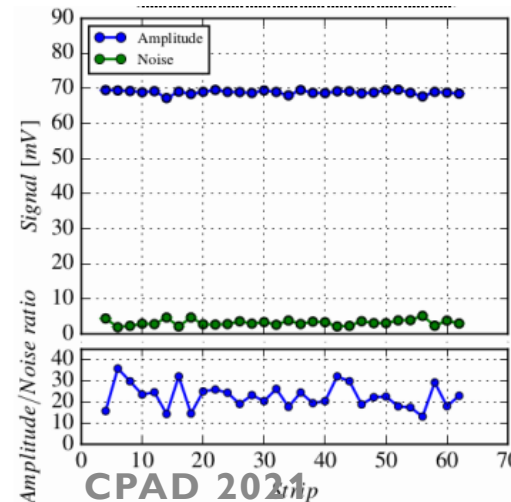
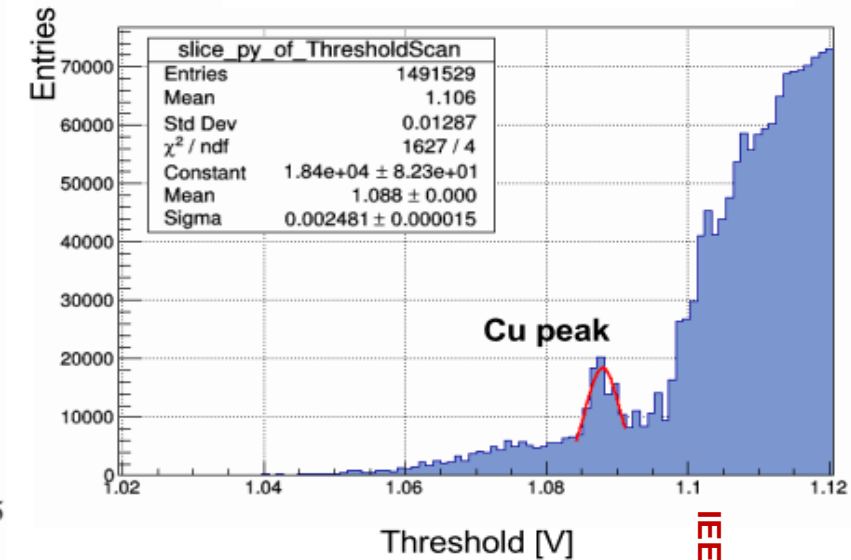
UNIVERSITY OF
BIRMINGHAM

- Cu x-ray spectrum measured with DECAL
- Unfocused laser spot and shaper output measured digitally
- Expected signal: $8050\text{eV} / 3.6\text{eV} = 2236\text{ e}$
 - calibration = $2236\text{ e} / 70\text{ mV} \approx 32\text{ e/mV}$
- Taking width of fitted peak as estimator of noise gives Signal/Noise ≈ 22
 - \Rightarrow Noise $\approx 100\text{ e}$

Energy spectrum of Cu measured with RAL HEXITEC detector



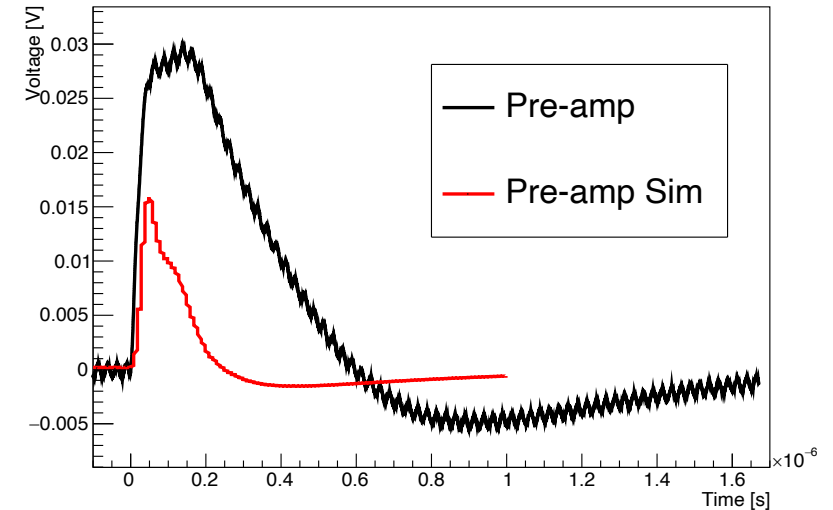
Scan of single strip threshold at which comparator first fires



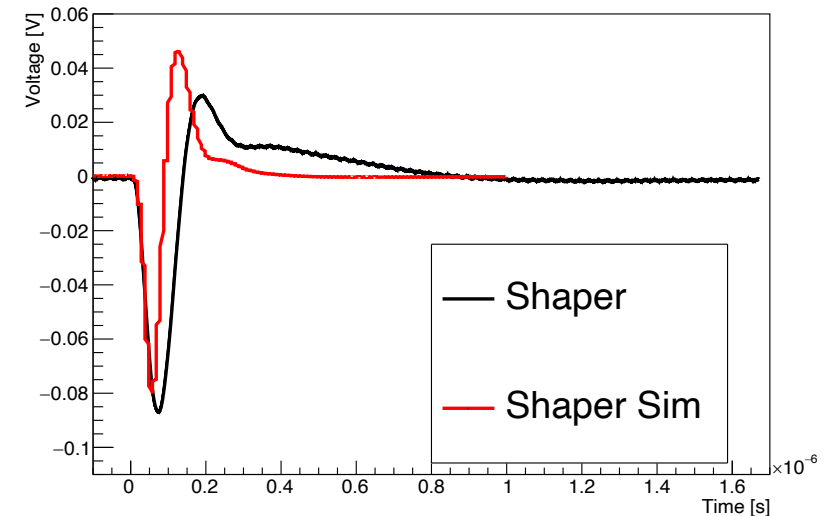
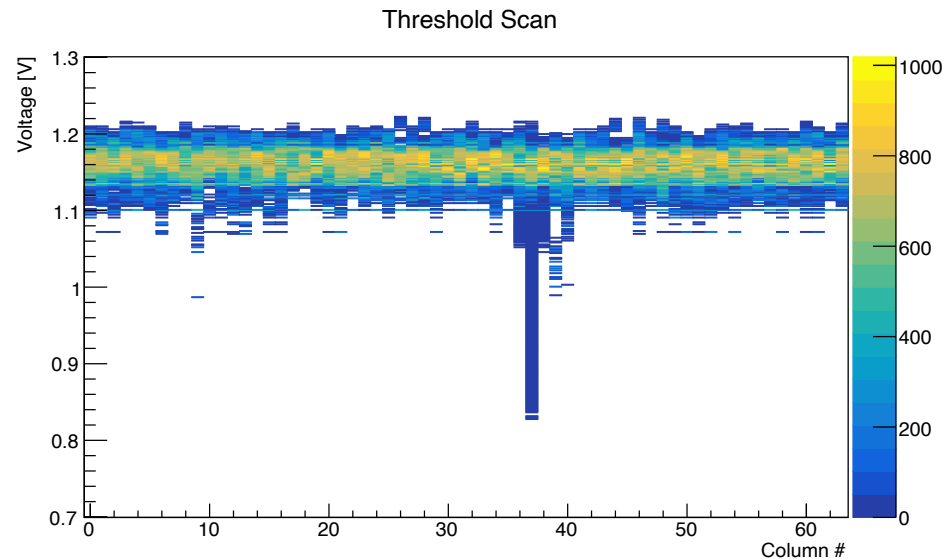
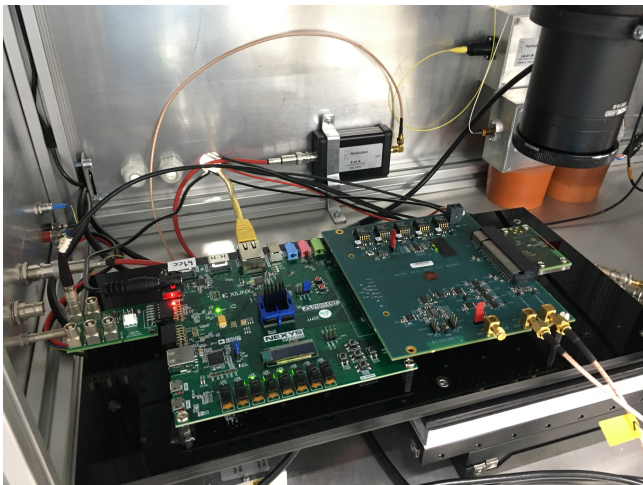
IEEE MIC-NSS (30/10/19) I. Kopsalis

DECAL FD laser measurements

- Measurement of analog test pixel with Particulars Large TCT system
- 1064 nm IR laser injected from backside
- Comparison to simulation with 2500 e⁻ input charge (roughly matches Cu calibration)
 - Rise time matches, but still a bit to be desired
- Digital pixels show response to laser in a threshold scan



Setup

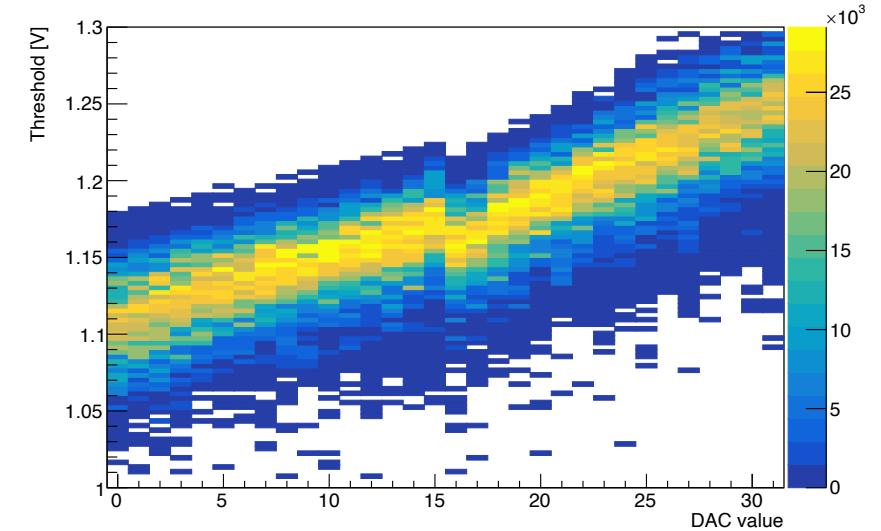


DECAL FD digital measurements

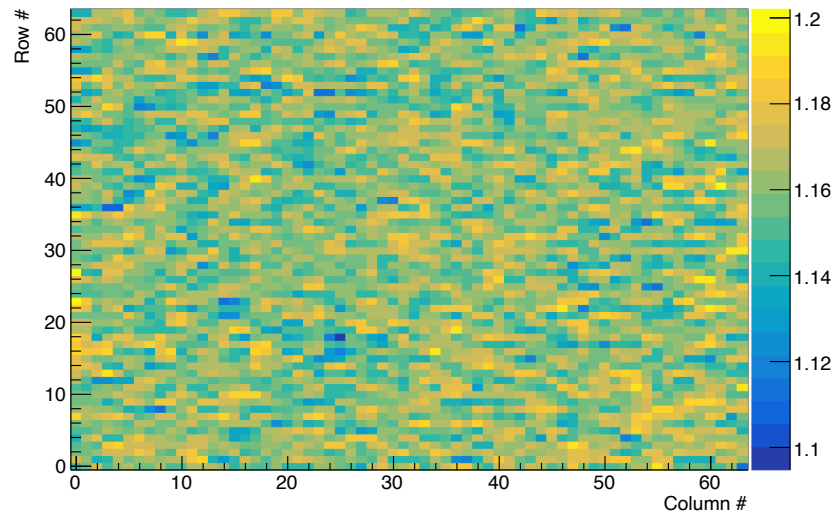
- With the DECAL FD chip bug fix to allow configuration of all columns
 - Can measure threshold in single pixels to make a threshold map and in principle tune the pixel matrix
- Scan of DACs shows good linearity with a kink in the center due to the trimming bit for the threshold polarity
 - ~150 mV of threshold trimming to tune pixels

DAC scan

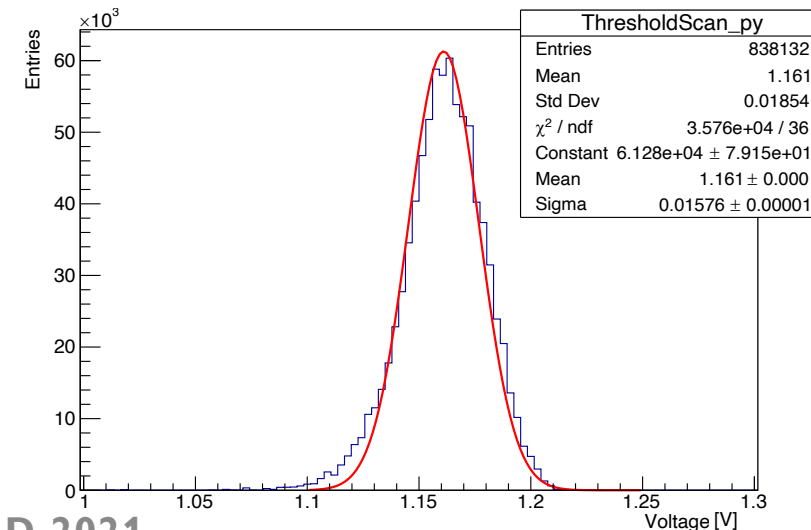
Threshold Scans vs. DAC



Threshold Map



Threshold Distribution



Summary

- A digital SiW calorimeter is being explored as a tool for future colliders that can provide high granularity for particle flow algorithms
- Simulation results show a comparable energy resolution for analog and digital SiW calorimeters up to 300 GeV
 - Simulated $\pi^0 \rightarrow \gamma\gamma$ reconstruction is on-going
- The DECAL FD prototype has been produced and is currently being tested
 - The sensor is fully configurable and digital and analog sectors are responsive; MIP testing, biasing studies, and irradiation planned

Summary

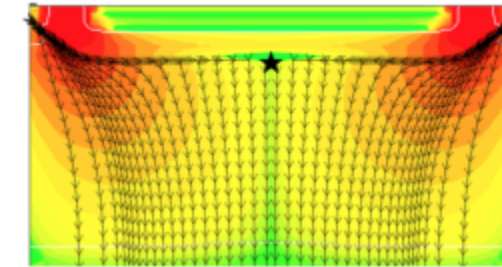
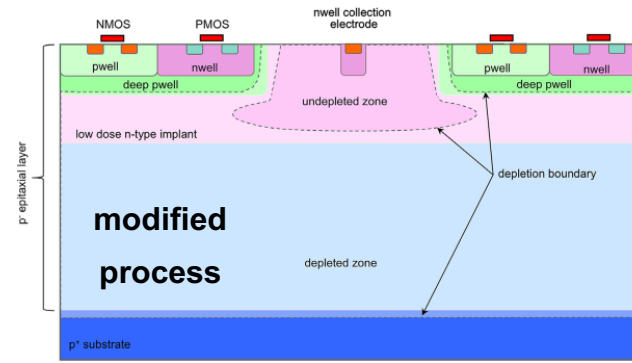
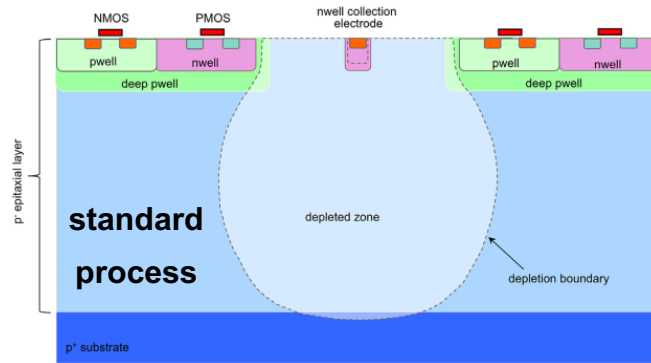
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Backup

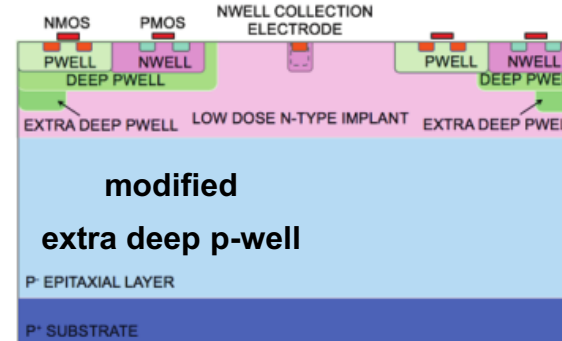
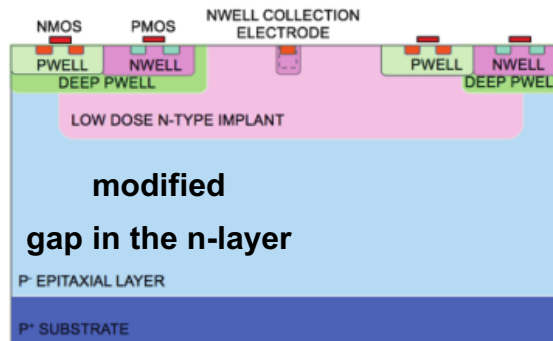
- Backup slides

TowerJazz Modified Process

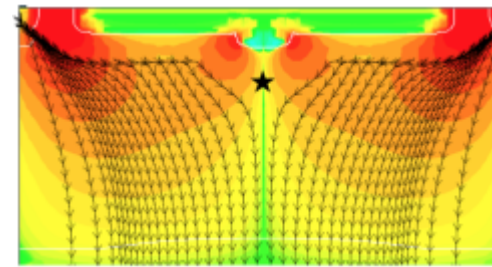
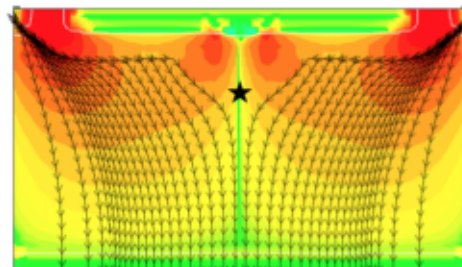
- The first version is referred to as an addition continuous n⁻ layer design for each pixel
- The second version consists of two variants (gap in the n- layer and extra deep p-well)
- expect shape of the electric field such that charge carriers are steered more directly towards the collection electrode in the pixel center



W. Snoeys et al., A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance, Nucl. Inst. and Meth. A 871 (2017) 90-96

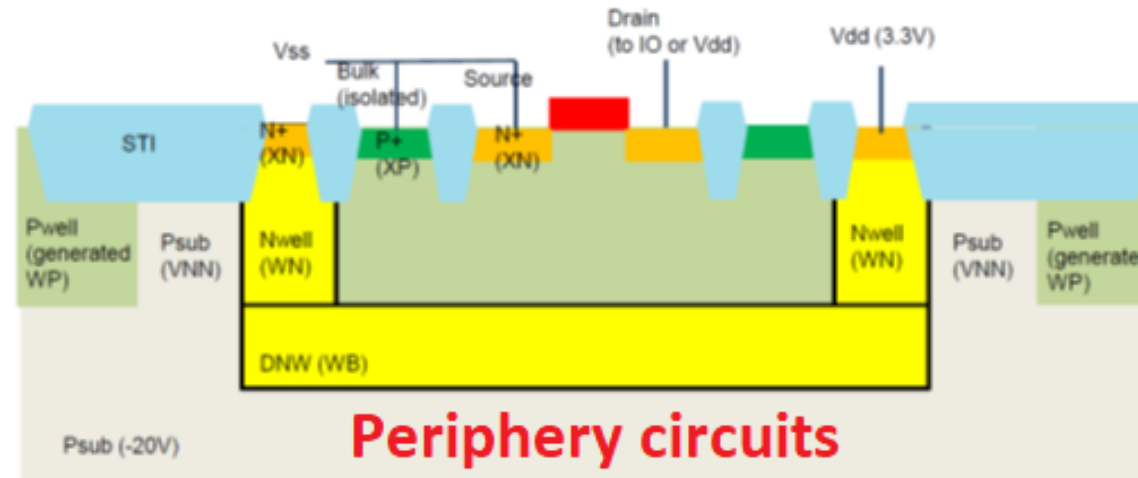
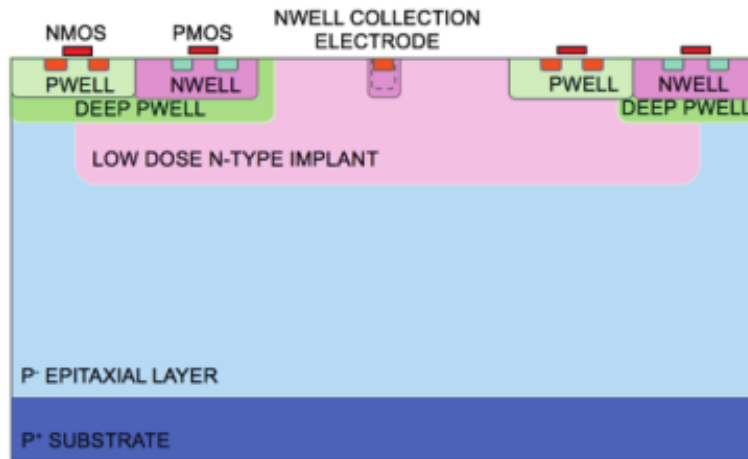


H. Pernegger, Depleted CMOS sensors for HL-LHC, Proceeding of Science, (VERTEX 2018), (041), 2018



M. Munker et al., Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance, Journal of Instrumentation 14 (2019) C05013

- The second version and the variant with the gap in the n⁻ layer was chosen



- Buried well (VWB) necessary to isolate the ground 0V from the substrate bias of -20V
- All n-well inside the same WB will be connected to the same supply
- A minimum spacing of 5 μm between two different WB is required
- The use of n-well capacitors or any n-well elements connected to ground is not possible

- Necessary modifications in the sensor design
- Pixel:
 - Fix problem report
 - Fully depleted layer with gap is the design goal
- PLL: Significant layout modifications
- LVDS drivers: Significant layout modification
- Pad ring: Major modifications (new library cells + FD modifications)
 - Create 1 pad for HV bias
 - Create 1 pad for -20V substrate
- Guard ring: Moderate layout modification
- Top level: Required significant layout modification on Y axis

